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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7257 Total Pages 2

First Named Inventor or Application Identifier Lior Horwitz

Express Mail Label No. EL143568193US

jc530 U.S. PTO
09/516337
03/01/00

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

09516337 030100

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 15)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 9)

4. ___ Oath or Declaration (Total Pages___)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
___ b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: _____

_____

_____

_____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
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or

X Correspondence Address Below

NAME Seth Z. Kalson, Reg. No.40,670

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

Docket No. 42390.P7257

Application for United States Letters Patent

for

Discharging Envelope Detector

by

Lior Horwitz

Noam Avni

and

Simoni Ben-Michael

DOCKET: 7257.5960

"Express Mail" mailing label number: EL143568193US
Date of Deposit: March 1, 2000
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3/1/00
(Date signed)

Seth Z. Kalson
Intel Corporation

Field

The present invention relates to analog circuits, and more particularly, to an envelope detector circuit for use in a communication system.

Background

The Home Phoneline Networking Alliance (HomePNA) is an incorporated, non-profit association of companies working to bring networking technology to the home. See www.homepna.org. HomePNA envisions bringing Ethernet technology to the home by utilizing existing home phone wiring for the network physical medium. HomePNA provides specifications for the physical layer (PHY), its interface to an Ethernet MAC (Media Access Control), and its interface to the home phone wiring. See the IEEE (Institute of Electrical and Electronic Engineers) 802.3 standard for Ethernet.

The position of a HomePNA PHY in relationship to the OSI (Open Systems Interconnection) model is illustrated in Fig. 1. Logical Link Control (LLC) **102** and MAC **104** are implemented in accordance with IEEE 802.3, and HomePNA PHY **106** communicates with MAC **104** via interface **108**. Additional sublayers, and other optional layers, may be added to the layers shown in Fig. 1 so that PHY **106** may provide services to other communication protocols, such as Gigabit Ethernet. In practice, PHY **106** and MAC **104** may be integrated on a single die, so that interface **108** is not readily visible.

PHY **106** receives a MAC frame from MAC **104**, strips off the 8 octets of preamble and delimiter from the MAC frame, adds a HomePNA PHY header to form a HomePNA PHY frame, and transmits a PHY frame on physical medium **108**. Fig. 2 illustrates HomePNA PHY framing. A PHY frame comprises Ethernet Packet **202**, and appended to Ethernet Packet **202** is a HomePNA PHY header, comprising SYNC interval **204**, Access ID (Identification) **206**, Silence interval **208**, and PCOM field **210**.

A PHY frame is transmitted on physical medium **108** utilizing pulse position modulation (PPM). All PHY symbols transmitted on physical medium **108** comprise a pulse formed of an integer number of cycles of a square wave that has been filtered with a bandpass filter. The position of the pulse conveys the transmitted symbol. Differential signaling is employed, in which a pulse and its negative are transmitted on two wires for each transmitted symbol. However, for simplicity of discussion, we consider only one component of the differential signal when describing the signal waveform.

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As indicated in Fig. 2, transmission begins with SYNC symbol 0, and Access ID field **206** is coded into seven AID (Access ID) symbols. SYNC symbol 0 may also be denoted as AID symbol 0. Access ID symbols 1 through 4 are used to identify individual stations to enable reliable collision detection. Access ID symbols 5 and 6 are used to transmit remote control management commands. AID symbol 7 is a silence interval.

SYNC symbol 0 and each AID symbol are 129 tics long, where 1 tic is defined as $(7/60)10^{-6}$ seconds, which is approximately 116.667 nanoseconds. AID symbols 1 through 7 begin with a blanking interval of 60 tics, followed by a pulse positioned within one of four time slots to convey two bits of information. The time slots are separated by 20 tics, and are at positions 66, 86, 106, and 126 tics from the beginning of an AID symbol interval. SYNC symbol 0 is composed of a SYNC_START pulse beginning at tic = 0 and a SYNC_END pulse beginning at tic = 126.

In the example of Fig. 2, AID symbols 1 through 4 represent the Access ID word 00101101, where AID symbol 1 represents AID0 = 1 and AID1 = 0, AID symbol 2 represents AID2 = 1 and AID3 = 1, AID symbol 3 represents AID4 = 0 and AID5 = 1, and AID symbol 4 represents AID6 = 0 and AID7 = 0. AID symbols 5 and 6 represent the control word 0001, where AID symbol 5 represents Ctrl0 = 1 and Ctrl1 = 0, and AID symbol 7 represents Ctrl2 = 0 and Ctrl3 = 0.

A collision is detected only during AID symbols 0 through 7. If a transmitting station reads back an AID value that does not match its own, then a collision is indicated, and a JAM signal is transmitted to alert other stations. Non-transmitting stations may also detect non-conforming AID pulses as collisions. Only a transmitting station emits a JAM signal.

Examples of transmitted and received pulses for three AID symbols are indicated in Figs. 3 and 4, respectively. In Fig. 4, SYNC_START and SYNC_END pulses indicate AID symbol 0. AID symbol 1 comprises a pulse in position 1 (tic = 86), and AID symbol 2 comprises a pulse at position 2 (tic = 106). A receiving PHY performs full-wave rectification of a received signal, and compares the envelope of the rectified signal with an AID slice threshold. The PHY detects a received pulse if its envelope exceeds the AID slice threshold. As soon as a pulse is detected by a PHY, the PHY disables further indications of detection until a time AID_END_BLANK (located at tic = 61) from the

beginning of the pulse, after which detection indication must be re-enabled for the next received pulse.

As indicated in Fig. 2, the data symbols in a PHY frame comprise two receiver training symbols, PCOM symbols, and symbols coding Ethernet packet **202**. (PCOM symbols are reserved for future use to be used by a local management entity, and are ignored by the PHY.) Referring now to Fig. 5, a data symbol interval begins with the beginning of a pulse, which defines tic = 0 for the symbol interval. Symbol timing (in tics) is measured from tic = 0. Except for the first data symbol interval, the beginning of a data symbol time interval is marked by the position of the pulse for the previous data symbol. The position of a pulse relative to the beginning of its time interval conveys the symbol information. Each position is separated by one tic. When a pulse begins transmission, the previous symbol interval ends and a new one immediately begins. Time intervals for data symbols are therefore variable, depending upon the transmitted data.

For example, as shown in Fig. 5, the beginning of the first data symbol interval is indicated by START_TX_PULSE at tic = 0, and the information conveyed by Data Symbol 1 is indicated by the position of Pulse 1 in Fig. 5. Pulse 1 then defines the beginning of the time interval for the next data symbol, Data Symbol 2.

Data receive timing is indicated in Fig. 6. In the example of Fig. 6, data symbol intervals for Data Symbol 1 and Data Symbol 2 are illustrated. The received waveform is formed from the transmitted pulse, along with any distortions and reflections that occur in the wiring network. The PHY detects the point at which the envelope crosses a threshold, denoted by Data_Slice_Threshold. Immediately after threshold detection, the PHY disables indication of detection for a time period END_DATA_BLANK, which is equal, in tics, to pulse position number 0 minus 3. Detection indication is enabled after END_DATA_BLANK.

Thus, as indicated in Figs. 4 and 6, a HomePNA PHY requires proper envelope detection of received waveforms. Envelope detection usually involves full-wave rectification followed by integration, where the integration is often performed by charging a capacitor. However, noise spikes on the home telephone network may lead to detection error. A detection error may result in inaccurately estimating pulse position (timing jitter), leading to incorrect symbol decoding. A detection error may also result in

a detection being declared when no pulse was actually transmitted by another station, i.e., a false alarm. A detection error may also result in the failure to declare a detection when a pulse was in fact transmitted.

Using large capacitors for signal integration may reduce detection error. Furthermore, in many prior art envelope detectors, the integrating capacitor is always being discharged by a discharge resistor. However, this type of discharging may cause output ripple, which may lead to timing jitter or an increase in the false alarm rate. Using a large capacitor, or providing for a longer discharge time, may reduce ripple.

However, using large capacitors, and using long discharge times, lead to various problems. In custom VLSI (Very Large Scale Integration) technology, large capacitors are expensive in terms of die area. Furthermore, the integrating capacitor should be discharged before the next arriving pulse, otherwise a slow discharging time may lead to detection error. Embodiments of the present invention address these problems, and are well suited to network communication utilizing home phone wiring as envisioned by the Home Phoneline Networking Alliance.

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Brief Description of the Drawings

Fig. 1 illustrates the position of a HomePNA PHY within the OSI communication protocol stack.

Fig. 2 illustrates HomePNA PHY framing.

Fig. 3 illustrates waveforms and timing for three transmitted Access ID symbols.

Fig. 4 illustrates waveforms and timing for three received Access ID symbols.

Fig. 5 illustrates waveforms and timing for two transmitted data symbols.

Fig. 6 illustrates waveforms and timing for two received data symbols.

Fig. 7 is a high-level circuit according to an embodiment of the present invention.

Fig. 8 is a more detailed circuit according to the embodiment of Fig. 7.

Fig. 9 is a high-level circuit according to another embodiment of the present invention.

Description of Embodiments

Fig. 7 provides a high-level circuit model of an embodiment of the present invention. Capacitor **702** is an integrating capacitor that is charged by current sink **704**. Current sink **704** is a voltage controlled current sink responsive to input voltage V_{in} at

input terminal (or port) **706**. Input voltage V_{in} may be a differential input voltage, although only one terminal to current sink **704** is explicitly shown. Input voltage V_{in} is the voltage propagated on physical medium **108** (the home phone lines) and received by a PHY.

Current sink **704** performs full-wave rectification, so that when a pulse is received by the PHY, the current drawn (sunk) at node **708** by current sink **704** is indicative of the rectified received pulse. While capacitor **702** is being charged, pMOSFET **710** (p-Metal Oxide Semiconductor Field Effect Transistor) is OFF. Because capacitor **702** serves as an integrator, the voltage at node **708** is indicative of the envelope of the received pulse when capacitor **702** is being charged by current sink **704**.

Transistor **714**, along with current mirror transistors **716** and **718** biased by a reference current I_{ref}, comprise a high input impedance buffer to sample the envelope voltage at node **708**, so that the output voltage, V_{out}, at node **720** is indicative of the envelope voltage at node **708**. Capacitor **722** serves as a lowpass filter, and resistors **724** and **726** serve as a voltage divider to provide a DC voltage level shift.

When the output voltage V_{out} at node **720** exceeds a threshold (e.g., AID_Slice_Threshold during the AID portion of the received PHY frame, or Data_Slice_Threshold during the data symbol portion of the received PHY frame), signal line DSCRG_ENV_L connected to the gate of pMOSFET **710** is switched LOW so that pMOSFET **710** is switched ON to discharge capacitor **702**. With pMOSFET **710** switched ON, pullup pMOSFET **712** acts as a voltage controlled current source to node **708**, so that the potential difference across capacitor **702** is reduced, thereby discharging capacitor **702**.

Using pullup pMOSFET **712** to discharge capacitor **702** provides for faster discharging than using a discharge resistor, thereby providing for a low detection error. However, it is found that for the HomePNA networking environment, in many instances V_{out} drops too low (it has an inverted spike) if capacitor **702** is discharged too quickly by pullup pMOSFET **712**, and this may cause signal interference with other circuit elements of the PHY. To remedy this problem, current sink **728** is provided.

Current sink **728** is connected to node **708** via serially connected transistors **730** and **710**. Transistor **730** is switched ON by setting HIGH signal line EN_FINE_DSCRG.

With EN_FINE_DSCRG set HIGH, current sink **728** is enabled in the sense that it sinks current from node **708** to ground when DSCRG_ENV_L is switched LOW.

Suppose current sink **728** is enabled (EN_FINE_DSCRG set HIGH). As the voltage at node **708** is brought lower due to capacitor **702** being charged by current sink **704**, pullup pMOSFET **712** switches ON and supplies drain current to current sink **728** via nMOSFET **730**. When DSCRG_ENV_L is switched LOW due to the voltage V_{out} at node **720** exceeding a threshold (e.g., detection of a pulse), the voltage at node **708** starts to rise as capacitor **702** is being discharged by pMOSFET **712**. Because the gate of pMOSFET **712** is connected to node **708**, the rising voltage at node **708** causes pMOSFET **712** to conduct less drain current. This results in a larger fraction of the current being sunk by current sink **728** to be drawn from capacitor **702**, so that the discharge rate of capacitor **702** is slowed down. The net effect of pMOSFET **712** in combination with current sink **728** is to allow for a "fine" discharge of capacitor **702**, so that the output voltage V_{out} transitions from a high level indicative of capacitor **702** being charged to a low level indicative of capacitor **702** being discharged without having an inverted spike.

Fig. 8 provides a more detailed circuit of the embodiment of Fig. 7, where like numerals among Figs. 7 and 8 denote similar circuit components. A differential voltage input signal is applied to input terminals **802** and **804**. The circuit components within dashed box **806** comprise a differential amplifier, providing a differential output voltage on lines **808** and **810**, and an output voltage on line **812**.

The circuit components within dashed boxes **704** and **728** serve as voltage-controlled current sinks, and are controlled by the voltages on lines **808**, **810**, and **812** so as to provide current sinks indicative of $|V_H - V_L|$, the magnitude of the difference between the input voltages at input terminals **802** and **804**. As indicated in Fig. 8, voltage-controlled current sink **702** is comprised of the differential transistor pair **850** and **852** cascaded with current sink transistor **854**, and voltage-controlled current sink **728** is comprised of the differential transistor pair **856** and **858** cascaded with current sink transistor **860**. Thus, in Fig 7 current sink **728** may be a voltage-controlled current sink similar to that of current sink **704** in that the current sunk by current sink **728** is indicative of the full-wave rectified received waveform.

The circuit components within dashed box **814** provide a bias voltage to the current mirror transistors **816**, **818**, **820**, **822**, and **824**. Transistor **818** provides a bias current to transistor **826**, where transistors **826**, **828**, and **830** comprise a current mirror. Transistor **830** provides a bias current to transistor **832**. Transistor **832** biases transistors **834**, **836**, and **838**. With transistor **840** OFF (EN_DSCRG is HIGH), transistors **834**, **836**, and **838** provide current to current sink **704**. If transistor **840** is ON (EN_DSCRG is LOW), then transistors **834** and **836** are bypassed and transistor **838** supplies more current to current sink **704** than when transistor **840** is OFF. Supplying more current to current sink **704** will cause integrating capacitor **702** to be charged at a slower rate by current sink **704**, and thus EN_DSCRG allows for adjustment of the charging rate of integrating capacitor **702** due to current sink **704**.

As capacitor **702** becomes charged, it provides less current to current sink **704**. But as capacitor **702** charges, the node voltage at node **708** decreases, so that pMOSFET **842** supplies more current to current sink **704** so as to offset the reduction in current supplied by capacitor **702**.

Variations may be made to the described embodiments without departing from the scope of the claims concluding this specification. For example, another embodiment is illustrated in Fig. 9, which functions in similar fashion to that of Fig. 7, but where pulldown transistor **904** is used instead of pullup transistor **712**, and where current sources **902** and **910** are used instead of current sinks **704** and **728**. For the embodiment of Fig. 9, integrating capacitor **702** is charged by current source **902** when nMOSFET **906** is OFF. After capacitor **702** is charged such that the output voltage V_{out} exceeds some threshold, pulldown transistor **904** discharges capacitor **702** when nMOSFET **906** is switched ON. When nMOSFET **908** is switched ON, the combination of pulldown nMOSFET **904** with current source **910** helps to prevent spikes in the output voltage V_{out}, as described earlier regarding Fig. 7.

As is understood from the embodiments of Figs. 7 and 9, current sources may be used instead of current sinks. Consequently, in the claims concluding this specification, it is to be understood that the term "current source" may mean a current source or a current sink.

What is claimed is:

1. A PHY responsive to first and second voltages on a network medium, the PHY comprising:

a capacitor;

a first current source to charge the capacitor by conducting a first conduction current indicative of the magnitude of the difference of the first and second voltages; and

a transistor to discharge the capacitor for a discharge time interval by conducting a transistor conduction current, the transistor coupled to the capacitor so that the transistor conduction current decreases in magnitude as the capacitor discharges during the discharge time interval.

2. The PHY as set forth in claim 1, the capacitor having a voltage difference, wherein the transistor is a pullup pMOSFET having a gate voltage responsive to the capacitor voltage difference.

3. The PHY as set forth in claim 1, the capacitor having a voltage difference, wherein the transistor is a pulldown nMOSFET having a gate voltage responsive to the capacitor voltage difference.

4. The PHY as set forth in claim 1, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second conduction current source is coupled to the

transistor so that the fraction of the second conduction current used to charge the capacitor increases as the transistor conduction current decreases.

5. The PHY as set forth in claim 4, wherein the second current source comprises:

a differential pair of transistors; and

a current source transistor cascaded with the differential pair of transistors.

6. The PHY as set forth in claim 1, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second current source charges the capacitor only if the transistor is ON.

7. The PHY as set forth in claim 4, further comprising:

a second current source to charge the capacitor by conducting a second conduction current, wherein the second current source charges the capacitor only if the transistor is ON.

8. The PHY as set forth in claim 4, wherein the second conduction current is indicative of the magnitude of the difference of the first and second voltages.

9. An envelope detector to detect the envelope of a differential voltage signal, the envelope detector comprising:

a node;

a capacitor connected to the node, the node having a node voltage;

a first current source to charge the capacitor so that the node voltage is indicative of the magnitude of the differential voltage signal;

a transistor having a gate connected to the node;

a second current source coupled to the node; and

an output buffer coupled to the node to provide an output voltage indicative of the node voltage;

wherein if the output voltage crosses a threshold, the transistor and the second current source in combination are coupled to the node to discharge the capacitor.

10. The envelope detector as set forth in claim 9, wherein the second current source comprises:

a differential pair of transistors; and

a current source transistor cascaded with the differential pair of transistors.

11. The envelope detector as set forth in claim 9, wherein

the first current source is connected to the node to sink a first current from the node indicative of the magnitude of the differential voltage signal;

the transistor is a pMOSFET; and

the transistor and the second current source in combination are coupled to the node to source a second current to the node if the output voltage crosses the threshold.

12. The envelope detector as set forth in claim 11, wherein

the pMOSFET has a drain current;

the second current source conducts a conduction current; and

the magnitude of the drain current is equal to the sum of the magnitude of the second current and the magnitude of the conduction current.

13. The envelope detector as set forth in claim 12, wherein

the conduction current source is indicative of the magnitude of the differential voltage signal.

14. The envelope detector as set forth in claim 9, wherein

the first current source is connected to the node to source a first current to the node indicative of the magnitude of the differential voltage signal;

the transistor is a nMOSFET; and

the transistor and the second current source in combination are coupled to the node to sink a second current from the node if the output voltage crosses the threshold.

15. The envelope detector as set forth in claim 14, wherein

the nMOSFET has a drain current;

the second current source conducts a conduction current; and

the magnitude of the drain current is equal to the sum of the magnitude of the second current and the magnitude of the conduction current.

16. The envelope detector as set forth in claim 15, wherein

the conduction current source is indicative of the magnitude of the differential voltage signal.

17. A communication system comprising:

a network medium comprising home phone wiring; and

a PHY responsive to first and second voltages on the home phone wiring, the PHY comprising:

a node having a node voltage;

a buffer to provide an output voltage indicative of the node voltage;

a capacitor connected to the node;

a first current source to charge the capacitor by conducting a first conduction current indicative of the magnitude of the difference of the first and second voltages; and

a FET to discharge the capacitor for a discharge time interval by conducting a drain current, the FET having a gate voltage responsive to the node voltage.

18. The communication system as set forth in claim 17, further comprising:

a MAC, wherein the PHY provides to the MAC an indication of detection if the output voltage crosses a threshold.

19. The communication system as set forth in claim 18, further comprising:

a second current source coupled to the node, wherein the FET and the second current source in combination discharge the capacitor during the discharge time interval.

20. A method to communicate via home phone wiring, the method comprising:

propagating information on the home phone wiring using pulse position modulation;

charging a capacitor with a current indicative of the full-wave rectification of a received differential voltage signal on the home phone wiring, the capacitor having a charge voltage;

buffering the capacitor charge voltage to provide an output voltage; and

discharging the capacitor if the output voltage crosses a threshold by conducting drain current through a FET , wherein the FET has a gate voltage responsive to the capacitor charge voltage.

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Abstract

A receiver to detect pulses on a home phone wiring network using envelope detection. The receiver comprises an integrating capacitor charged by a first current source responsive to a differential signal propagated on the wiring network, and discharged by a FET in combination with a second current source. The combination of the FET and the second current source allows the capacitor to be quickly discharged in a smooth fashion. An application of this receiver is for a PHY according to the Home Phoneline Networking Alliance.

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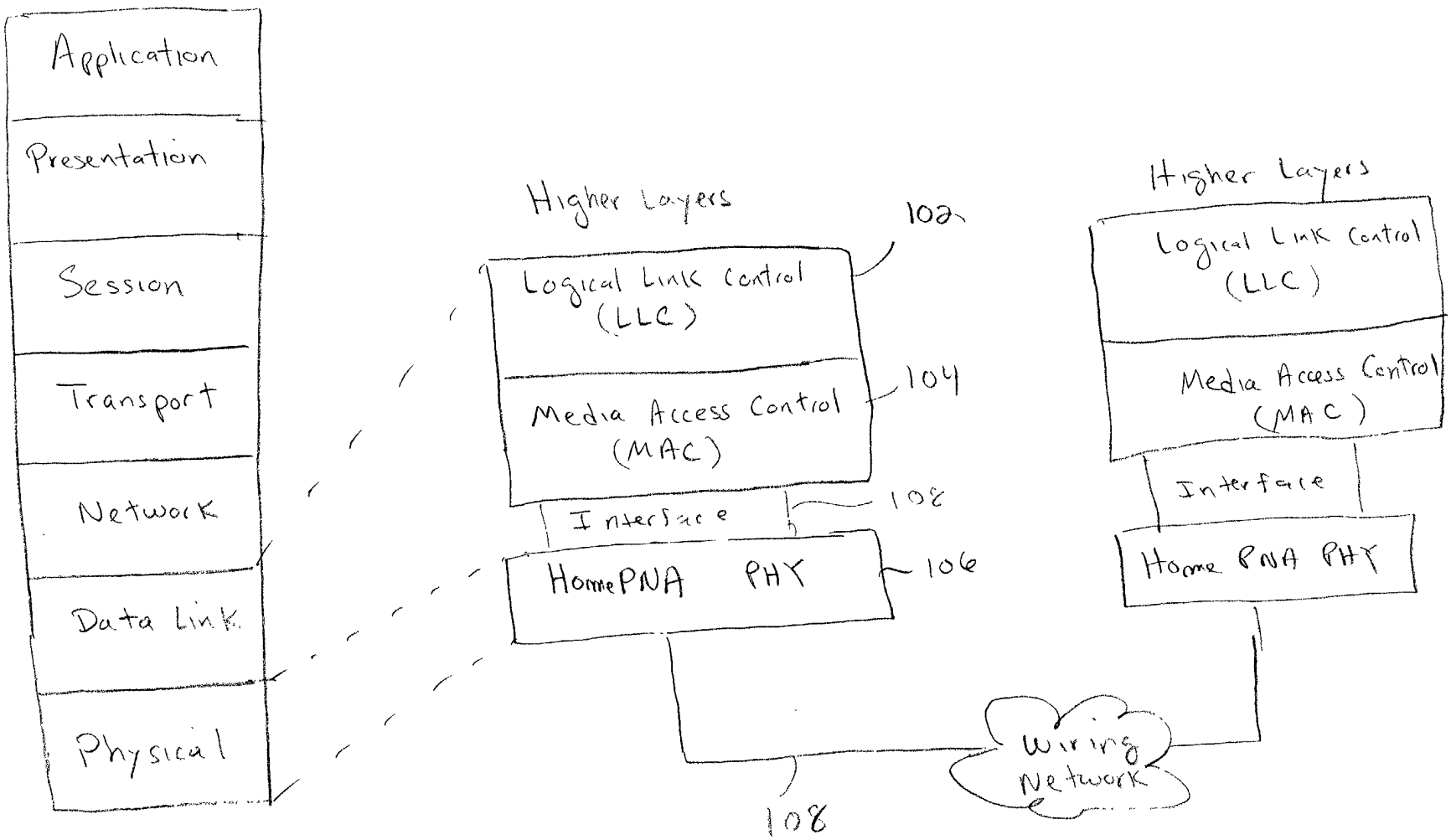


Fig. 1 (Prior Art)

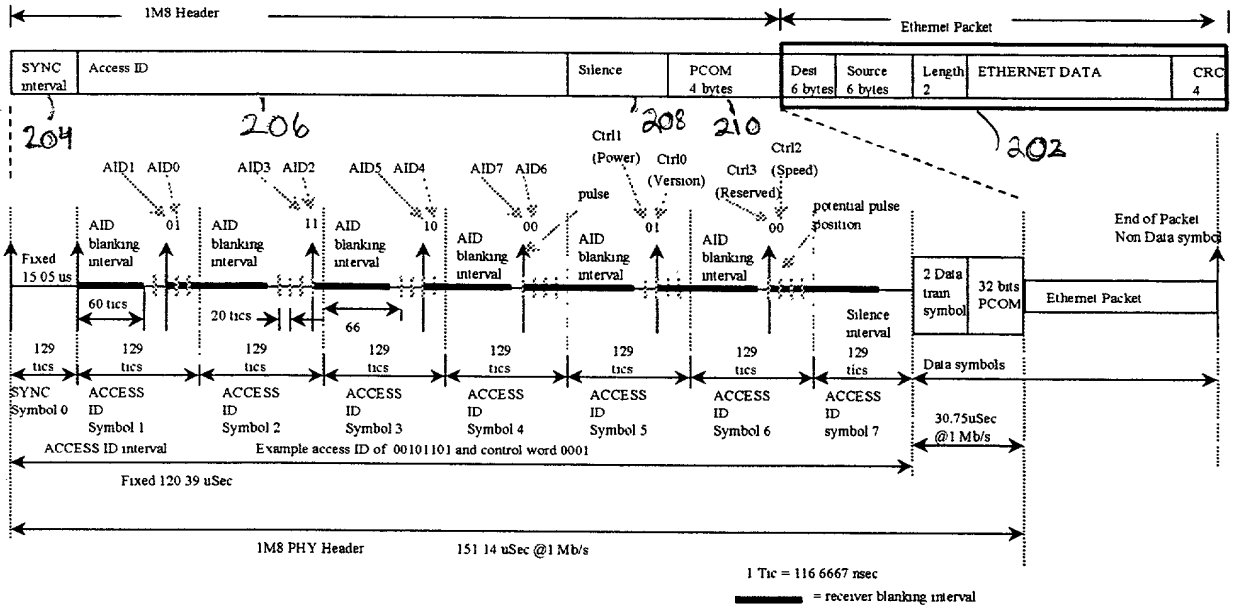
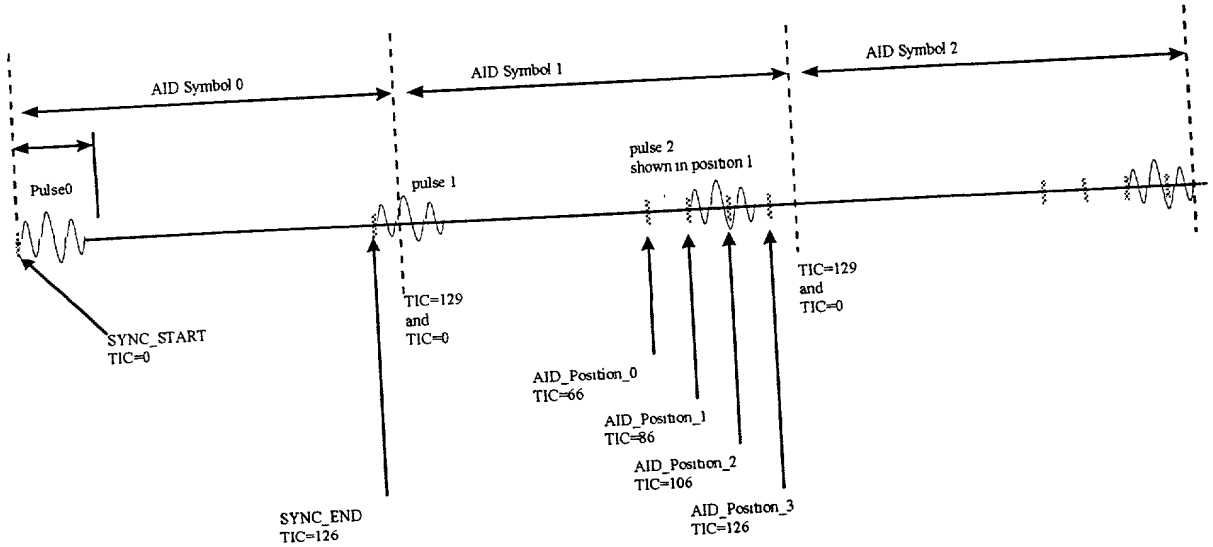


Fig. 2 (Prior Art)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AID Symbol 2
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TIC=0
TIC=129
and
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TIC=66
AID_Position_1
TIC=86
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AID_Position_3
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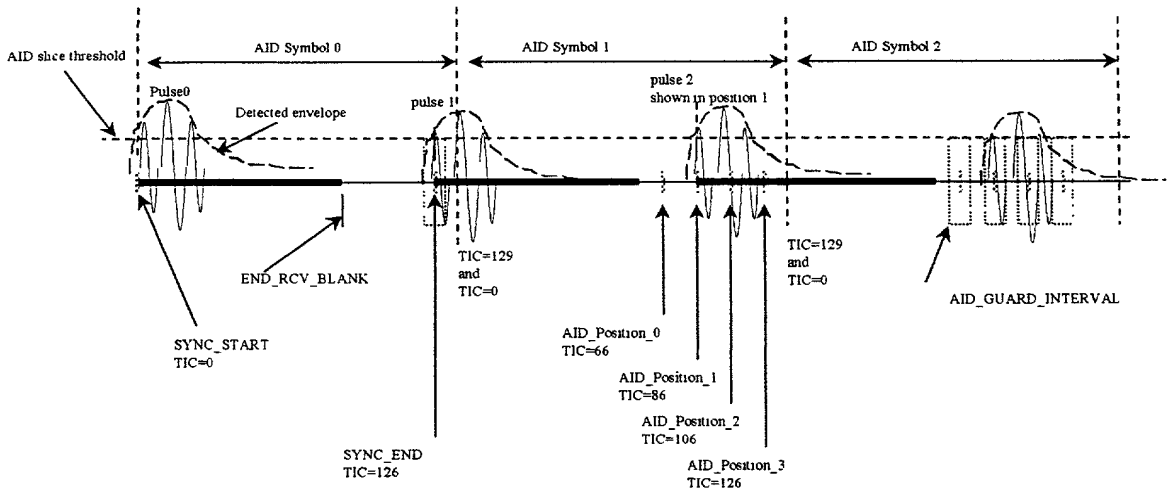
Fig. 3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AID Symbol 1
AID Symbol 2
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pulse 2
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and
TIC=0
TIC=129
and
TIC=0
AID_GUARD_INTERVAL
SYNC_START
TIC=0
AID_Position_0
TIC=66
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TIC=126
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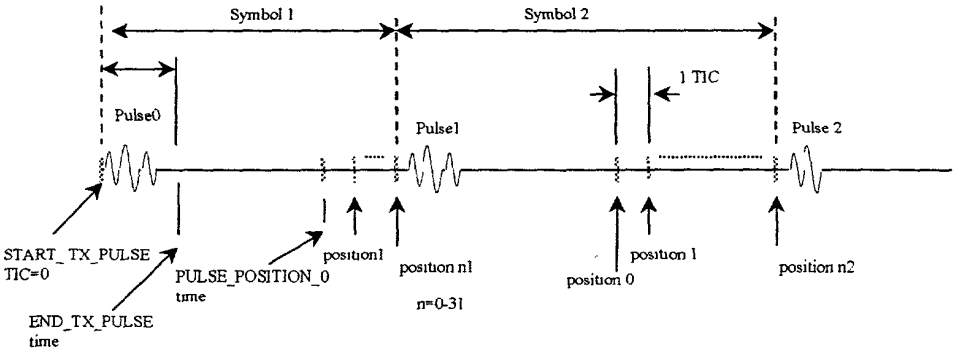
TIC=126

Fig. 4


Symbol 1
Symbol 2
1 TIC
Pulse0
Pulse1
Pulse 2
START_ TX_PULSE
TIC=0
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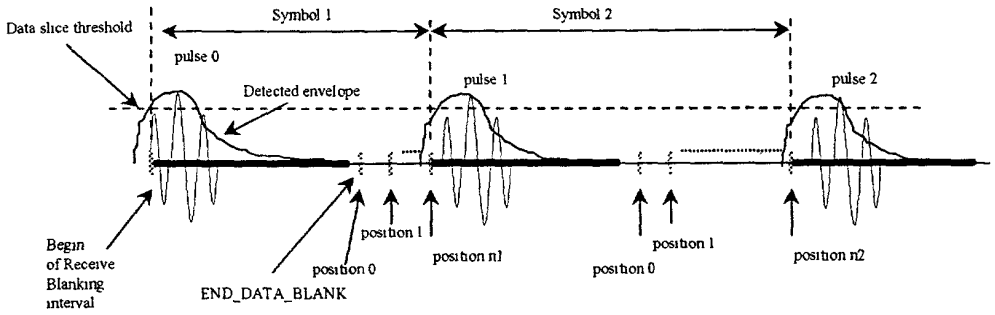
position n1
n=0-31
position 0
position 1
position n2
END_TX_PULSE
time

Fig. 5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Symbol 2
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Detected envelope
pulse 1
pulse 2
Begin
of Receive
Blanking
interval
END_DATA_BLANK
position 0
position 1
position n1
position 0
position 1
position n2

Fig. 6

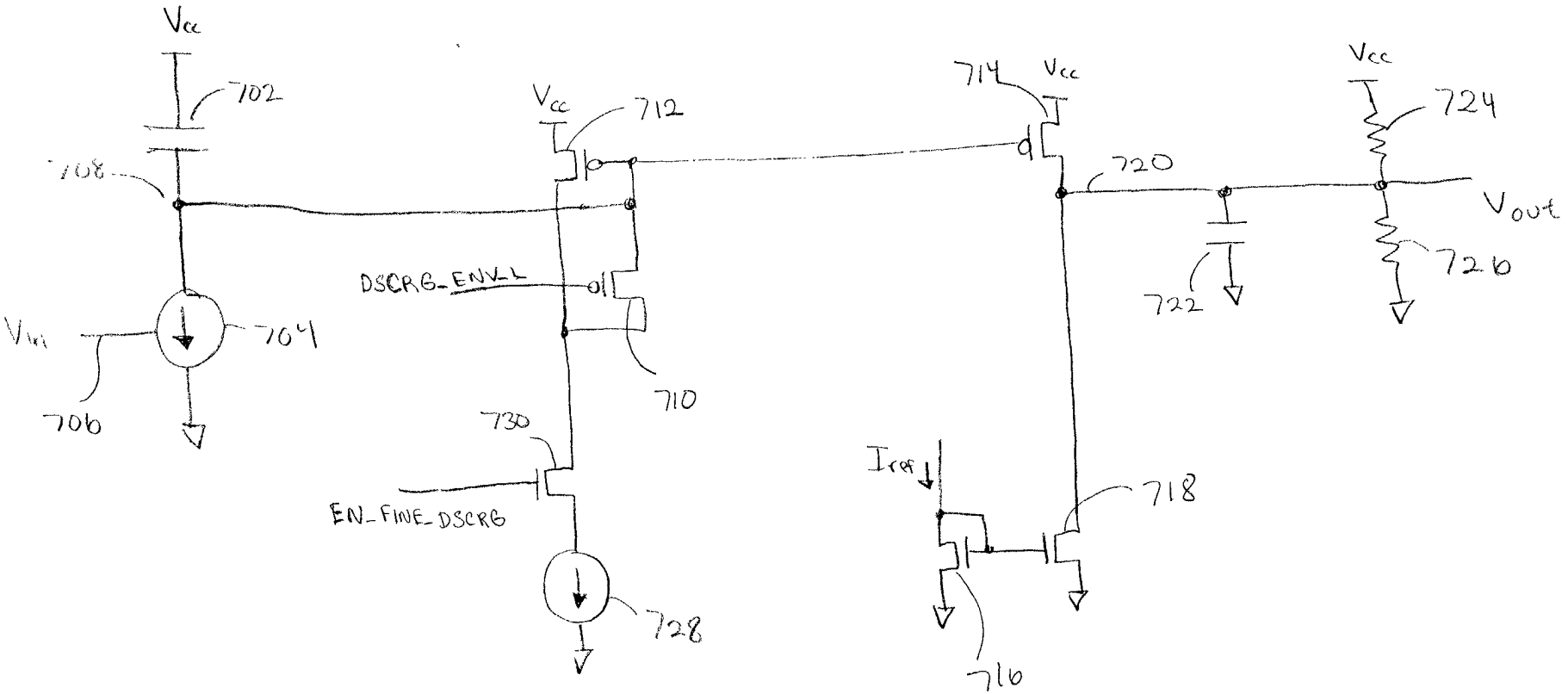
Vcc
702
708
Vin
704
706
DSCRG_ENVL
710
Vcc
712
730
EN_FINE_DSCRG
728
714
Vcc
720
Iref
718
716
722
Vcc
724
Vout
726

Fig. 7

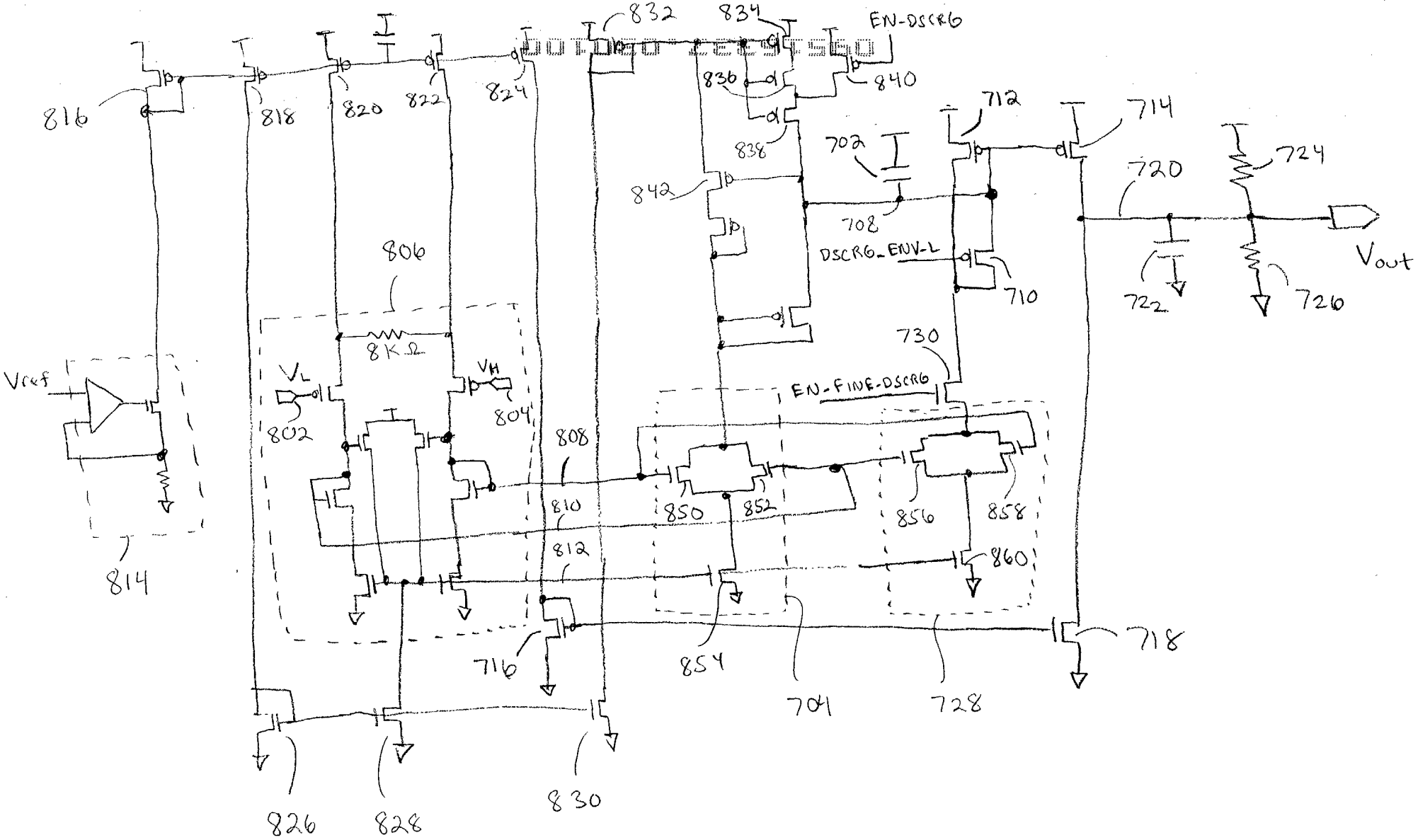
816
818
820
822
824
832
834
EN-DSCRG
836
840
838
842
712
714
702
720
724
708
DSCRG_ENV-L
710
722
726
Vout
806
8KΩ
Vref
VL
VH
802
804
808
730
EN-FINE-DSCRG
810
812
850
852
856
858
860
814
716
854
701
728
718
826
828
830

Fig. 8

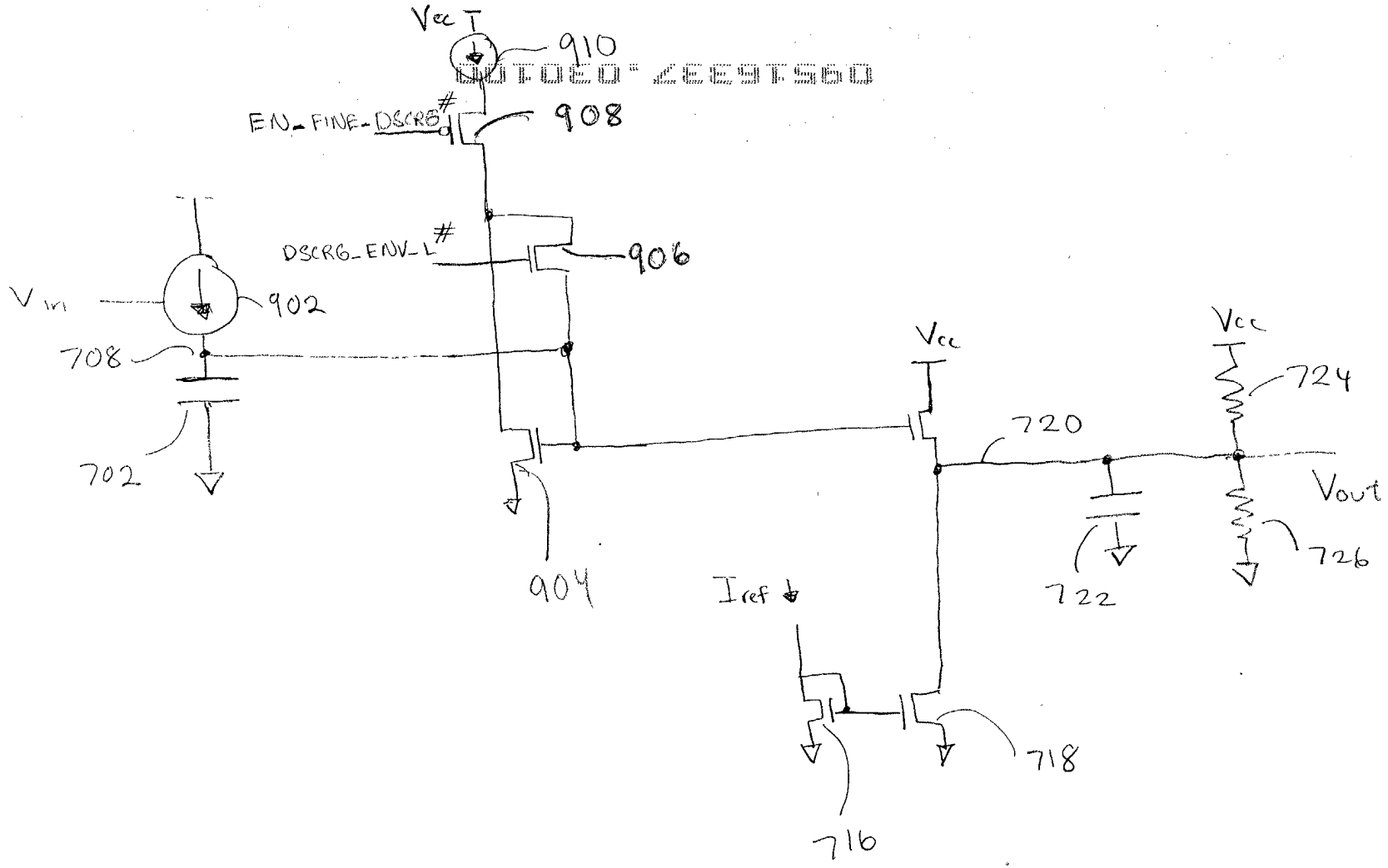
Vcc
910
EN_FINE_DSCRG#
908
DSCRG_ENV_L#
906
Vin
902
708
702
904
Vcc
720
Vcc
724
Vout
726
722
Iref
718
716

Fig. 9